Amendments to the Claims:.

1. (Currently Amended) A circuit comprising:

at least one delay element for receiving an input signal and for generating a time delay in said signal to produce a time-delayed signal;

calibration circuit, coupled to said delay element, for calibrating said delay element so as to match said time delay to a predetermined time period, said calibration circuit comprising a control loop for receiving an output signal from said delay element and a reference signal and for generating a phase adjustment based on a phase difference between said output and reference signals; and

multiplier-summing circuit, coupled to said delay element, for multiplying at least one signal output from said delay element to produce at least one multiplied signal and for summing at least one multiplied signal ~~multiplied~~ to generate an equalized signal.

2. (Currently Amended) The circuit as set forth in claim 1, wherein:

~~said calibration circuit comprises a control loop for receiving a reference signal, output from said delay element, and for generating a phase adjustment based on said delay of said reference signal propagated through said delay element; and~~

said delay element comprises selectable parameters for receiving a phase adjustment from said control loop and for setting said selectable parameters based on said phase adjustment.

3. (Currently Amended) The circuit as set forth in claim 2, wherein said control loop comprises:

phase detector for measuring ~~a~~ said phase difference between said reference and output signals ~~signal, input to said delay element, and a signal output from said delay element~~; and

loop filter, coupled to receive ~~said~~ a signal output from said phase detector, for generating said phase adjustment ~~based on a predetermined response of said phase difference~~.

4. (Canceled)

5. (Original) The circuit as set forth in claim 1, wherein said delay element comprises a transmission line.

6. (Original) The circuit as set forth in claim 5, wherein said delay element further comprises a means for adjusting capacitance for said transmission line, so as to calibrate said delay element.

7. (Original) The circuit as set forth in claim 1, wherein said delay element comprises lumped circuit elements .

8. (Original) The circuit as set forth in claim 7, wherein said delay

element further comprises a means for selecting combinations of said lumped parameters to calibrate said delay element.

9. (Currently Amended) The circuit as set forth in claim 1, wherein said delay element comprises a plurality of ~~(stub)~~ stub transmission lines.

10. (Original) The circuit as set forth in claim 9, wherein said delay element further comprises a means for selecting a length of said stub transmission lines to calibrate said delay element.

11. (Currently Amended) A method for filtering a signal, said method comprising the steps of:

receiving an input signal in at least one delay element;

generating a time delay in said signal to produce a time-delayed signal;

calibrating said delay element so as to match said time delay to a predetermined time period, wherein said calibrating comprises:

receiving an output signal from said delay element and a reference signal; and

generating a phase adjustment based on a phase difference between said output and reference signals;

multiplying at least one signal output from said delay element to produce at least one multiplied signal; and

summing at least one multiplied signal to generate an equalized signal.

12. (Currently Amended) The method as set forth in claim 11, wherein:

~~the step of calibrating said delay element comprises the steps of receiving a reference signal, output from said delay element, and for generating a phase adjustment based on said delay of said reference signal propagated through said delay element; and~~

the step of receiving an input signal in at least one delay element comprises the steps of receiving an input signal in a delay element that comprises selectable parameters, receiving a phase adjustment, and setting said selectable parameters based on said phase adjustment.

13. (Currently Amended) The method as set forth in claim 12, wherein the step of generating a phase adjustment comprises the steps of:

measuring ~~a~~ said phase difference between said reference and output signals ~~signal, input to said delay element, and a signal output from said delay element~~; and

generating said phase adjustment ~~based on a predetermined response of said phase difference~~.

14. (Canceled)

15. (Original) The method as set forth in claim 11, wherein said delay element comprises a transmission line.

16. (Original) The method as set forth in claim 15, further comprising the steps of adjusting capacitance for said transmission line, so as to calibrate said delay element.

17. (Original) The method as set forth in claim 11, wherein said delay element comprises lumped circuit elements .

18. (Original) The method as set forth in claim 17, further comprising the step of selecting combinations of said lumped parameters to calibrate said delay element.

19. (Currently Amended) The method as set forth in claim 11, wherein said delay element comprises a plurality of ~~(stub)~~ stub transmission lines.

20. (Original) The method as set forth in claim 19, further comprising the step of selecting a length of said stub transmission lines to calibrate said delay element.

21. (Canceled).

22. (Canceled).

23. (New) The circuit as set forth in claim 1, wherein:

said reference signal comprises said input signal; and

said output signal comprises said time-delayed signal.

24. (New) A circuit comprising:

at least one delay element for receiving a signal and for generating a time delay in said signal, said delay element comprising a transmission line and a means for adjusting capacitance for said transmission line for calibrating said delay element;

calibration circuit, coupled to said delay element, for calibrating said delay element so as to match said time delay to a predetermined time period; and

multiplier-summing circuit, coupled to said delay element, for multiplying at least one signal output from said delay element and for summing at least one multiplied signal to generate an equalized signal.